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TECHNICAL PAPER

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High aspect ratio air core solenoid inductors using an improved UV-LIGA process with contrast enhancement material

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Abstract In this paper, we investigate the application of a contrast enhancement material (CEM388SS®, Shin-Etsu MicroSi, Inc., AZ, USA) on thick SU-8 negative photoresist (Microchem Corp., MA, USA) and its use in the construction of a high aspect ratio on-chip solenoid inductor. Various SU8 test microstructures (with aspect ratio of 10:1 and 20:1) were "rst constructed by utilizing this improved UV-LIGA process to demonstrate the clear di erence before and after the application of CEM. It was found that this material dramatically reduced the ••T-topping•• e ect and improved the structural pro"le angle; and higher aspect ratio microstructures could be achieved without modi"cation/upgrades of any kind on the existing lithography tool. Furthermore, we implemented this process in the fabrication work of high aspect ratio air core solenoid inductor and obtained a very high quality (Q) factor of 72.8 at 9.7 GHz from a 3-turn inductors and a high inductance of 28 nH from a 20-turn inductor. Experimental data showed that inductors with taller via structures (higher aspect ratio) had better radio frequency (RF) characteristics than those of lower via structures, which are highly desirable in many communication applications.

1 Introduction

The rapidly growing wireless communication world has placed a series of demands on today•s radio frequency (RF) components to provide more functionality with higher portability at lower cost. In the observation of high phase noise and power consumption found in typical active semiconductor devices which are dedicated to perform RF functions, as well as high manufacturing cost if they were fabricated based on gallium arsenide (GaAs) technology, micromachined on-chip passive RF devices have been realized with the motivation to improve the above scenarios. Among these passive devices, high quality on-chip inductors have attracted enormous attention in the past decade since their small size, low power consumption and phase noise level are essential in constructing high performance LC tank and resonant circuitry and these components are highly desired in many RF applications. In recent years, three dimensional (3D) on-chip inductors have gained more popularity in the MEMS community since they have demonstrated high potential in executing RF roles in the terms of high quality (Q) factor and self-resonant frequency with very small chip area occupati7on (Kim and Allen 1998; Chomnawang et al. 2003; Chua et al. 2003).

The Q factor of an inductor could be represented in the simplest form as $Q = \omega L / R_s$, where ω is the operating frequency and L is the coil inductance. The parameter R_s represents the equivalent series resistance of the coil, which strongly depends on operating frequency due to skin e ect and proximity e ect, as well as conductor•s material and geometry. Therefore, to achieve higher Q factor at high frequency, the inductance of a coil should be maximized and meanwhile, the total capacitance and the equivalent series resistance of the coil should be minimized. The total capacitance produced by a coil at high frequency is generally considered to consist of two parts, which include substrate-to-conductor (substrate parasitic e ects) and conductor-to-conductor capacitance (stray capacitance).

The inductance of a conventional long solenoid inductor could be represented in the simple form as $L = N^2 tw\mu / l$, where N is the number of windings, t, w, l, and μ represent the height, width, length, and permeability of the inductor core, respectively. Therefore, a high aspect ratio structure ($t > w$) is desirable in achieving high inductance within a given two dimensional (l, w) area. In our three layer (bottom conductor,

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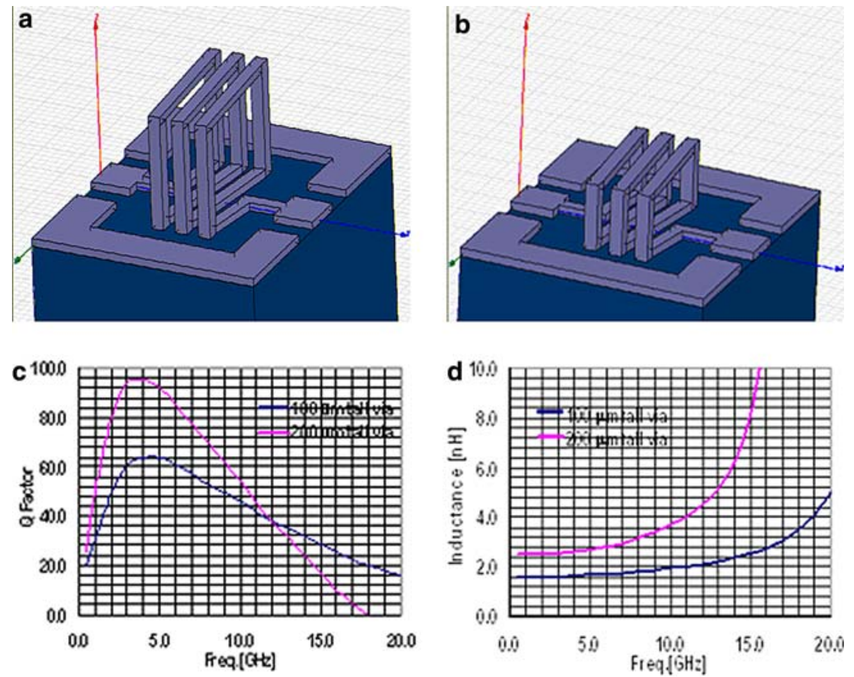

Fig. 1 HFSS simulation: a schematic of a 3-turn inductor with 200 μm tall via; b same design with 100μm via; c simulated Q factor plots for the two inductors; and d simulated inductance plots for the two inductors

via structure, top conductor) solenoid inductor, taller via structure would o er the advantage in enlarging the core area and consequently producing higher inductance within the given chip area, which is a key factor in producing higher Q factor based on the earlier equation. To verify the above assumption, we simulated proposed solenoid inductors at high frequency using Ansoft HFSS® software and the result showed that as other geometrical parameters (inductor core width, conductor dimension, pitch distance, etc.) remained the same, inductor with taller via structure held better Q and higher inductance than that those with lower via structure, as shown in Fig. 1.

The creation of microstructures with higher aspect ratio has always been a major interest and challenge in the MEMS research community. Among various techniques, the combination of UV photolithography with high contrast photoresist such as SU-8 has been proven

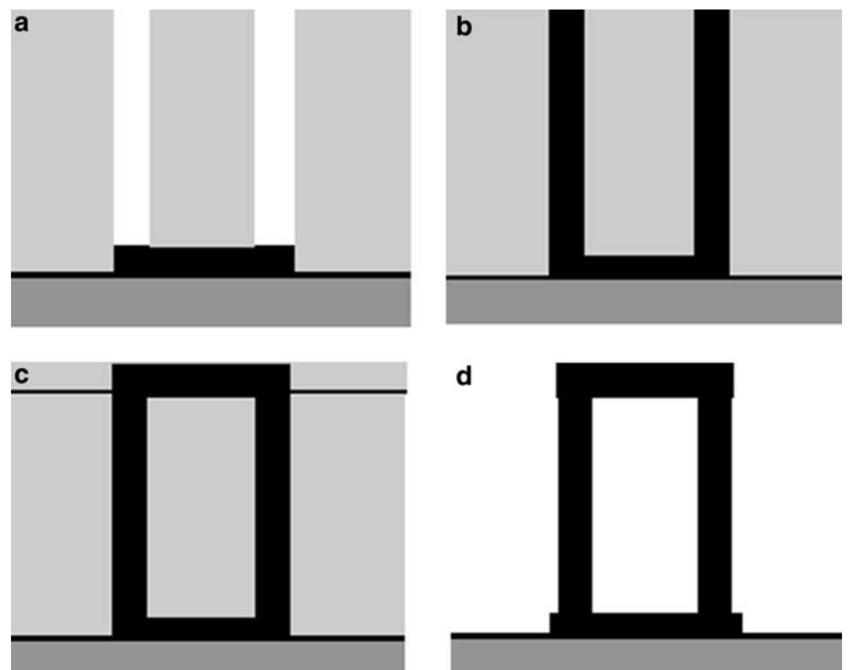

Fig. 2 Air core high aspect ratio solenoid inductor fabrication sequence a bottom conductor and via mold formation; b via structures construction; c top conductors formation; and d SU-8 mold and metal seed layer removal

to be an e ective and economical surface micromachining technology in constructing high aspect ratio microstructures (Lorentz et al. 1997, 1998; Zhang et al. 2001). However, the structure•s maximum aspect ratio that can be achieved using this method is constrained by the equipment capability (i.e., exposure power, UV source intensity and wavelength, etc.) and further improvement usually requires certain modi“cations/upgrades to the existing tool.

In this work, we proposed and fabricated a variety of air core high aspect ratio solenoid inductors with the primary goal to obtain high Q factor, high inductance and self-resonant frequency within small chip area utilizing an SU-8 based, improved UV-LIGA process. This process, which is simple to implement, remarkably enhanced the lithography performance of the available system and more importantly, did not involve any modi“cation/upgrade to the existing exposure tool.

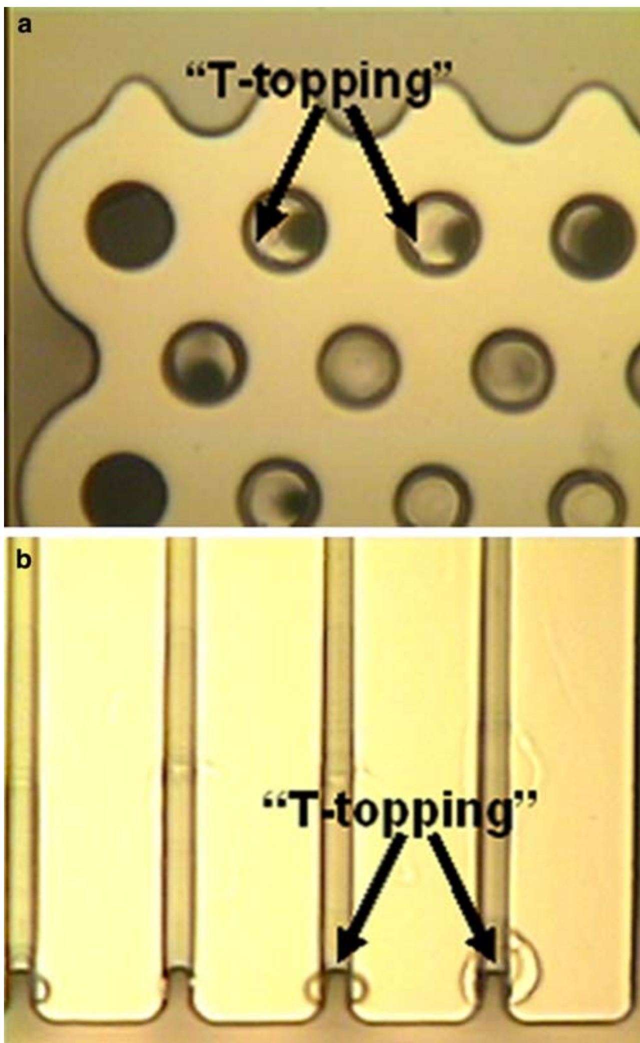

Fig. 3 ••T-topping•• e ect appeared during long exposure time of thick SU-8 photoresist in: a deep hole structures; and b deep narrow trench structures

2 Experiment

Inductors are fabricated on a 3″ diameter high-resistivity ($\rho \approx 10^{10}$ Ω/cm) low-dielectric-constant ($\varepsilon_r \approx 4.6$) 700 μm thick Pyrex glass wafer. As illustrated in the process ”ow (Fig. 2), this square cored solenoid inductor consists of three layers„bottom conductor, via structure, and top conductor. A seed layer is “rst sputtered to form the electroplating base and then a 20 μm thick SU-8 bottom conductor mold is created by photoresist spin-coating and UV lithography. Followed by copper electroplating to form the bottom conductors, another layer of SU8 (100 ~ 200 μm in thickness) is spun onto the “rst layer and via structures are completed with the same UV patterning and electroplating techniques. After top seed layer sputtering, the top conductors are “nished in the same way as the bottom conductors. Finally, SU-8 mold layers and metallic seed layers are removed by plasma dry etch (20% CF_4 : 80% O_2) and wet chemical etch, respectively.

During inductor fabrication, the formation of deep via mold presented the most demanding and challenging task among all the processing steps. As mentioned earlier, the maximum aspect ratio of a microstructure that can be achieved by standard UV lithography is generally limited by the equipment capacity. Large UV dose which is necessary to fully expose the thick photoresist would induce a phenomenon so called ••T-topping•• e ect, as shown in Fig. 3; that is, a thin solid crust observed at the top of the structures after the development process, which is suspected to be caused by the heat generated at the interface between the mask and the photoresist due to the long exposure time. This undesirable feature sometimes could become severe and di cult to remove; which directly affects the further process steps such as electroplating in the deep trench/hole mold. Although various methods have been recommended to reduce such e ect, for example, installing optical “lter to cut down the UV wavelength (SU-8: A thick photoresist for MEMS, http://www.aveclafaux.freeservers.com/SU-8.html), and dividing long exposure time into short intervals (http://www.geocities.com/guerinlj/), ••T-topping•• remained a

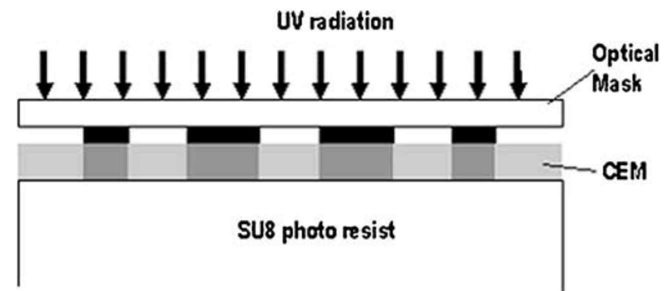

Fig. 4 Schematic drawing of contrast enhancement material (CEM) functioning as a ••conformal contact mask•• during UV exposure

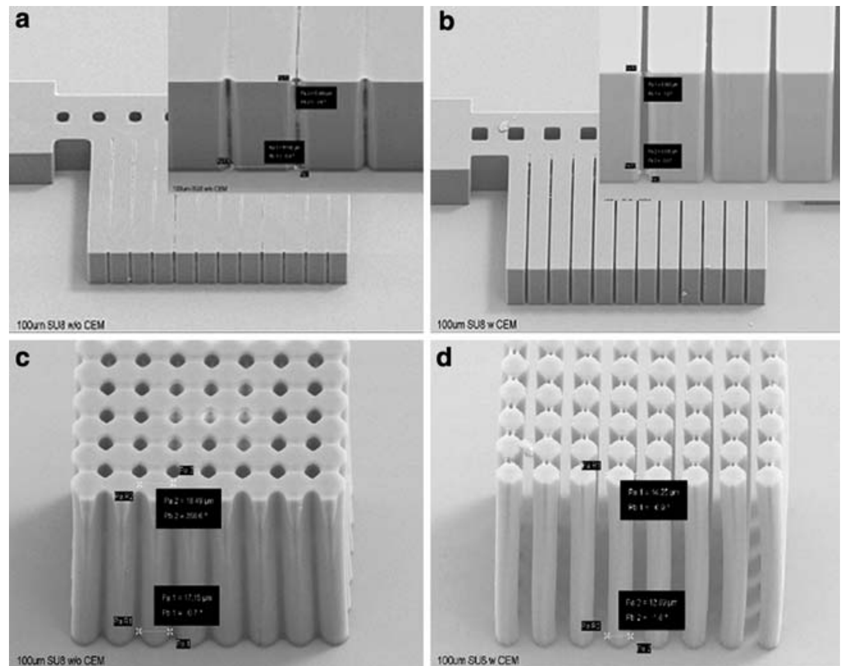

Fig. 5 SEM microphotograph of 100 μm thick SU-8 test structures: a and b samples prepared without CEM; c and d samples prepared with CEM

di cult issue to overcome as the photoresist thickness increased.

Contrast enhancement material (CEM) has been widely studied and applied in the past decade in conventional IC industry to gain better resolution (smaller critical dimension) in photolithography process (Halle 1985; Mack 1987; Hirai et al. 1987; Chiong et al. 1989). In recent years, people have reported the deployment of CEM on di erent positive photoresists in MEMS-based researches and obtained satisfactory results (Flack et al. 2004; Miyajima and Mehregany 1995). However, the implementation of such material on ultra thick negative tone photoresist, to our knowledge, has not yet been attempted.

The CEM used in our study (CEM388SS) is designated for thick (20 μm or thicker) photoresist applications. This product is a photo bleachable solution which is initially opaque to the UV or near UV wavelength (350…405 nm) but becomes nearly transparent upon exposure. As shown in Fig. 4, CEM spun onto the sample prior to the UV exposure functions as a ••conformal contact mask•• which e ectively lowers the light scattering between the mask and the photoresist.

During exposure, CEM in clear areas of the optical mask bleaches at a much faster rate than in covered areas and the adjustment of the bleaching dynamics results in a higher contrast level of the aerial image in the mask. The advantage of CEM is that it is simple to apply (conventional spin coater) and does not require a separate solvent to strip,,it is a water soluble material and therefore a thorough DI water rinse after UV exposure will complete the removal.

The CEM process is explained in detail below: after standard SU-8 soft bake,

1. Spin coat barrier coat (BC 7.5) layer at 4,000 RPM for 30 s. The purpose of barrier coat is to prevent any potential intermixing between CEM and the photoresist. Dry in air for 4…5 min.
2. Spin coat CEM388SS at 2,000 RPM for 30 s, dry in air for 4…5 min before UV exposure. Incompletely dried CEM layer may cause SU-8 sticks to the mask. It also should be noted that drying CEM too long (> 10 min) will degrade the performance of the material.
3. UV exposure. Due the absorption of CEM and barrier coat layer, it typically requires 30…50% more UV dose than original recipe to fully expose SU-8, depends on photoresist thickness.
4. Strip CEM and barrier coat layers by gentle DI water rinsing (25…30 s), then gently blow the sample dry with nitrogen gas.
5. Standard post exposure bake and developing.

Figure 5 shows SU-8 sample microstructures (100 μm thick) prepared with and without CEM388SS.

As can be seen from the photos, CEM had a clear impact on exposure resolution and the sample exposed with CEM experienced much less ••T-topping•• e ect and exhibited much steeper side wall, and smaller dimensional change than those of the samples prepared without CEM. Figure 6 shows a comb “nger structure mold made with CEM that had deep trench mold with an aspect ratio approximately 20:1 and a calculated pro“le angle of 89.34°.

The material and the process have been tested repeatedly and showed consistent performance in improving the exposure quality and reducing ••T-topping•• e ect. We then implemented such process in our

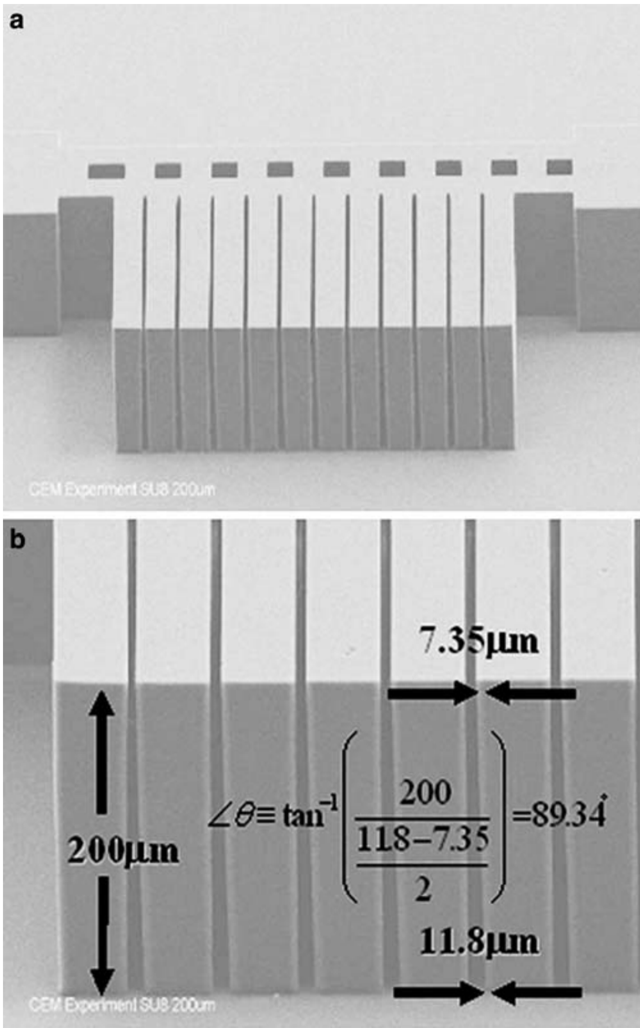

Fig. 6 SEM microphotograph of 200 µm thick SU-8 comb “nger con“guration with ~ 20:1 deep trench structure and a calculated structural pro“le angle of 89.34° a overall view, and b enlarged view

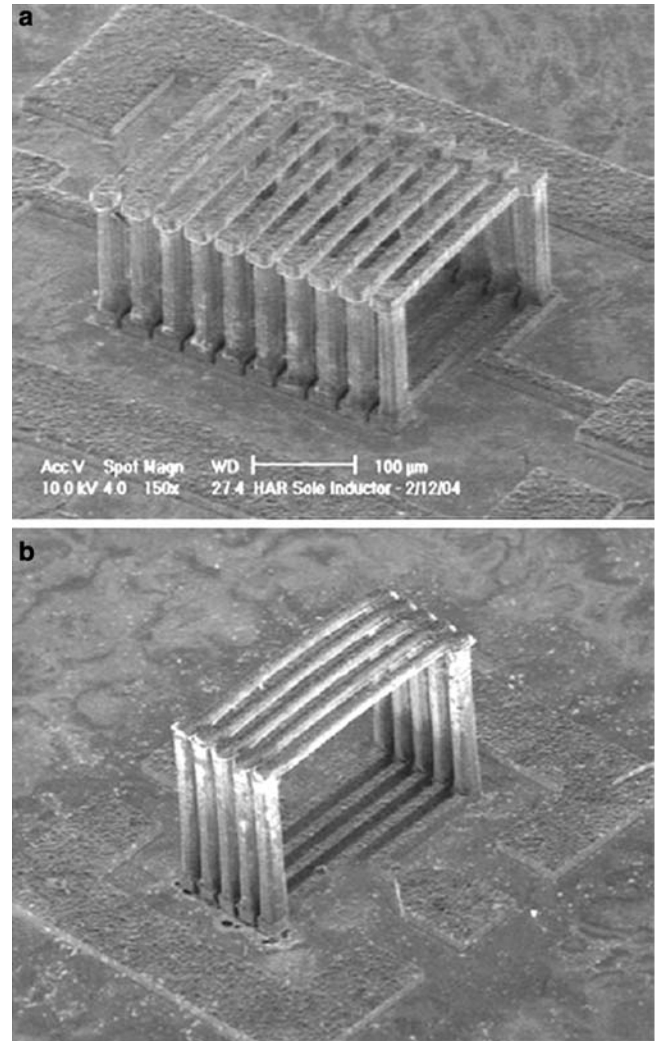

Fig. 7 SEM microphotograph of fabricated solenoid inductor with a 100 µm tall via structure, with an aspect ratio of 5:1; and b 200 µm tall via structure, with an aspect ratio of 10:1

solenoid inductor fabrication and successfully constructed inductors with 100 and 200 µm tall via structures, as shown in Fig. 7; achieving structure aspect ratios 5:1 and 10:1, respectively.

3 Characterization and discussion

Fabricated inductors with di erent via height were measured by Anritsu 37369A vector network analyzer with a Cascade Summit 12k on-wafer probing system. First, the Cascade HPC150 ground-signal-ground (GSG) probes were calibrated using a Cascade 114-456A calibration substrate. The calibration method used was Load…Re”ect…Re”ect…Match (LRRM) using Cascade WinCal software v2.30 and the S-parameter data was captured using the same software in the frequency sweep range from 0.4 to 40 GHz. The parasitic e ects induced by signal pads and ground plane were subtracted from overall measurements with de-embedding procedure to ensure the accuracy of the “nal results. Y-parameter data were extracted from the measured S-parameter data using the method explained in Arcioni et al. (1998) and inductors• major RF characteristics are calculated as following:

$$Q = \frac{\mathrm{Im}[1/Y_{11}]}{\mathrm{Re}[1/Y_{11}]}, \tag{1}$$

$$L = \frac{\mathrm{Im}[1/Y_{11}]}{\omega}. \tag{2}$$

The highest Q factor that we obtained was 72.8 at 9.7 GHz, which was produced by a 3-turn inductor with 200 µm tall via structures. It occupied an area of 0.03 mm^2. This inductor had an inductance value of 2.15 nH at peak Q frequency, and self-resonant frequency of 31 GHz. The highest inductance that we obtained was 28 nH at peak Q frequency of 2 GHz by a

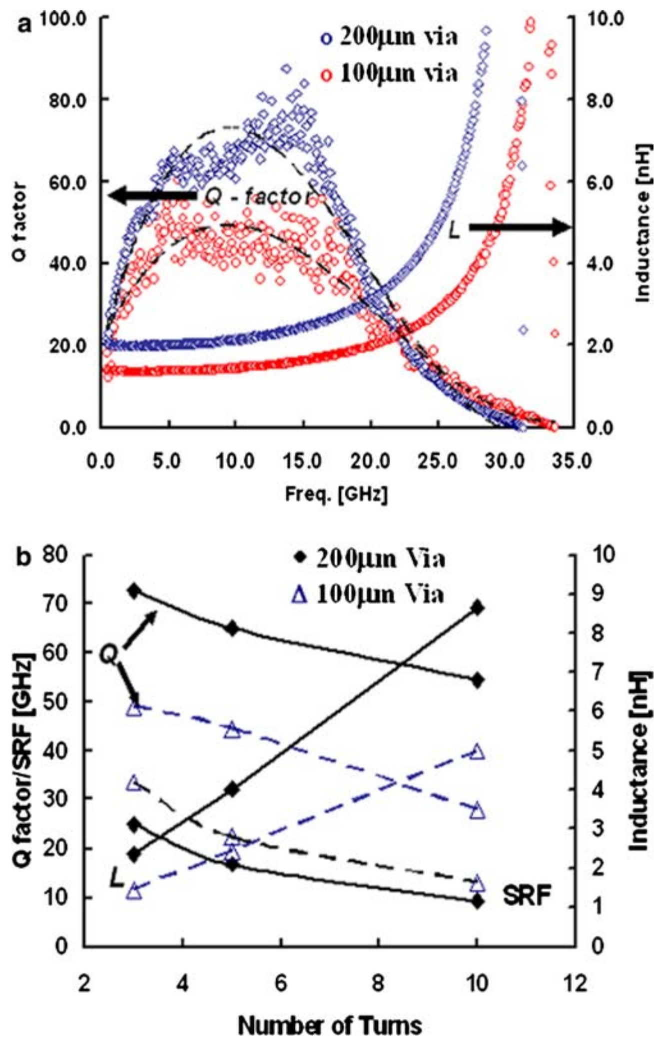

Fig. 8 Measurement data of a high frequency response of a 3-turn inductor with 100 and 200 μm via structures; and b trend plots of major RF characteristics for the same inductor groups with di erent via structure heights

20-turn inductor 200 μm tall via structures. This inductor occupied 0.75 mm^2 in area and held a peak Q factor of 43 and a self-resonant frequency of 5.1 GHz.

Measurement results showed that while other geometrical parameters remained the same, inductors had taller via structure (higher aspect ratio) held higher Q factors and inductances but lower self-resonant frequencies than those with lower via, which con“rmed the earlier HFSS® simulation results, as shown in Fig. 8a. Figure 8b shows the trend plot of major RF characteristics as a function of number of turns of one inductor group but with di erent via heights. The average percentage increase in Q was approximately 45% as via height increased from 100 to 200 μm. Inductances exhibit a linear relationship with number of turns; inductors with taller via possess steeper slope than that of inductors with shorter via. We believe that larger magnetic ”ux area resulted from taller via structures o ered stronger mutual coupling between windings and thus produced higher total inductance. This e ect is more obvious for inductors with more windings, as the percentage change in inductance increased from 50 to 73.5% for 3-turn and 10-turn inductors, respectively. Higher inductance consequently resulted in higher Q factors. The reason for relatively steady change in Q is suspected to be caused by higher resistance produced by taller via structures. In addition to the resistance growth, increased stray capacitance due to enlarged via-to-via area is likely to be another factor to restrict further growth of Q.

The two inductor groups had similar self-resonant frequency trends. As expected, self-resonant frequency dropped quickly as inductor consisted more turns. In addition to higher inductance produced by more windings, larger direct facing surface area among conductors and via structures, more importantly, bigger contact area with the substrate made inductors with more turns experience higher stray capacitance and substrate parasitic e ects and therefore held much lower self-resonant frequencies. Therefore, higher inductance and bigger stray capacitance produced by taller via structures should be the primary reason for higher aspect ratio inductors having lower self-resonant frequencies than those of shorter via inductors.

4 Conclusions

In this work, we realized an improved UV-LIGA process by investigating the application of CEM (CEM388SS) on thick SU-8 photoresist. We found this material/process dramatically improved the exposure resolution of SU-8 photoresist and higher aspect ratio microstructures could be achieved without modi“cation of any kind in the existing lithography tool. This improved process did not involve any dedicated equipment or material and provided consistent results. Furthermore, we successfully fabricated air core solenoid inductors with high aspect ratio via structures by using this process and attained impressive RF characteristics from them. Both simulation and experiment data veri“ed that inductors with taller via structure would possess better Q factors and higher inductances, which are highly desirable in many communication applications.

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